REMARKS

1. Claim Rejections – 35 U.S.C. 103(a)

Claims 1 – 4 and 6 – 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cho.

Response

Claim 1

Claim 1 has been amended to include limitations of claims 10 and 11. With regards to the 103 rejection of claims 10 and 11 as being unpatentable over Romano, upon careful review of Romano's disclosure, the applicant finds no description pertinent to graphics decoding for generating audio data and video data. Though Romano discloses using a single, monolithic integrated circuit embodying all or substantially all of the motion control and processing functionality associated with servo control of a disk drive [Col. 3, lines 1-4], the applicant respectfully asserts that forming a graphics decoding circuit on the same monolithic substrate on which the servo control components are formed is neither taught nor suggested by Romano. One of the objectives of the claimed invention is to provide a single integrated chip that provides both DVD-ROM controller functionality and MPEG decoder functionality [Para 0009]. The single integrated chip is referred to as "a monolithic/packing substrate". Therefore, the applicant respectfully asserts that a combined teaching of Cho and Romano fails to teach or suggest the claimed feature "the decoder circuit, **the graphics decoding circuit** and the memory controller are either fabricated on **a monolithic substrate or within a packaging substrate**" (*emphasis added*).

In the Office action dated 04/20/2007, the Examiner stated that Cho discloses an electronic circuit comprising a memory controller to provide read and write access to an

external memory for both a servo control and ECC decoder circuit and a graphics decoding circuit (1st memory controller 121 and 2nd memory controller 122 of Fig. 2), and it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two memory controllers into one memory controller. However, according to the arguments set forth hereinafter, the applicant respectfully points out that the memory controller and external memory of Claim 1 are neither taught nor suggested by the combined result indicated by the examiner.

The prior art system decoder in Cho's disclosure is for performing demodulation and ECC decoding before data is transmitted to the A/V decoder for following audio and video data decoding: "An A/V decoder interface and DVD-ROM interface 120 connected to the second data bus 127 transmits the descrambled data stored in the second memory **to** the audio/video decoder 600 and/or the ROM decoder 950" [Col. 2, lines 39-43]. Additionally, as depicted in Cho Fig. 2, the arrow symbol points out a **one-way direction** representative of a data outputting path to the external A/V decoder and/or the ROM decoder. Furthermore, upon careful review of Cho's disclosure, the applicant finds no description pertinent to using the second memory to buffer any data generated from the audio/video decoder. In other words, there is no need for the prior art audio/video decoder mentioned by Cho's disclosure to write data into the second memory through the second memory controller embedded in the preceding system decoder. In other words, the applicant respectfully notes that Cho's disclosure fails to teach or suggest allowing both the system decoder and the A/V decoder to write data into a shared external memory. Even though the two memory controllers (reference numerals 121 and 122 in Cho Fig. 2) might be integrated into one combined memory controller, the applicant respectfully notes that the combination result negates the need of providing the combined memory controller to grant write access to the external memory for the A/V decoder as using a shared external memory for buffering data **outputted from** the system decoder and **the A/V decoder** is against the teachings of Cho.

Moreover, the applicant disagrees with the statement that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine two memory controllers into one memory controller". The applicant wishes to cite *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983), in which Nortron argued that the invention of Schenck merely integrated a machine that had previously been made in four bolted pieces. The court found this argument unpersuasive and held that the claims were patentable because the prior art perceived a need for mechanisms to dampen resonance, whereas Schenck eliminated the need for dampening via the one-piece gapless support structure, showing insight contrary to the understandings and expectations of the art. In addition, MPEP 2142 states that, for an obviousness rejection, "the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination". By utilizing a single memory controller, the system disclosed in Claim 1 overcomes the need for two separate RAM banks and reduces complexity and cost of production. As the use of the single memory controller is not simply an engineering choice but yields benefits not anticipated by the teachings of the prior art, the applicant respectfully asserts that the use of a single memory controller would not be obvious to a person of ordinary skill in the art. Furthermore, as stated above, the use of the single memory controller enables the servo control and EDD decoding circuit and the graphics decoding circuit to write data into the shared external memory. Therefore, the applicant respectfully asserts that the single memory controller of Claim 1 overcomes the obviousness rejection.

In light of at least the reasons stated above, the applicant believes the claimed feature "a memory controller to provide read and **write access** to the external memory for both

the servo control and ECC decoder circuit and **the graphics decoding circuit**" is neither taught nor suggested by teachings of Cho (*emphasis added*). Reconsideration of Claim 1 is respectfully requested.

Claims 2 – 4 and 6 – 8

Claims 2 – 4 and 6 – 8 are dependent on Claim 1 and should be found allowable if Claim 1 is found allowable.

2. Claim Rejections – 35 U.S.C. 103(a)

Claim 9 was rejected under 35 U.S.C. 103a() as being unpatentable over Cho and Chau.

Response

Claim 9 is dependent on Claim 1 and should therefore be found allowable if Claim 1 is found allowable.

3. Claim Rejections – 35 U.S.C. 103(a)

Claims 5, 13 and 14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cho and further in view of Yuen et al.

Response

Claim 5

Claim 5 is dependent on Claim 1 and should therefore be found allowable.

Claims 13 and 14

Claim 13 has been amended to correct for erroneous dependency. Claims 13 and 14

are dependent on Claim 12. As the applicant believes Claim 12 should be found allowable over the prior art for reasons detailed in the following section, claims 13 and 14 should also be found allowable.

4. Claim Rejections – 35 U.S.C. 103(a)

Claims 10, 11 and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cho and further in view of Romano.

Response

Claim 10

Claim 10 has been cancelled, and its limitations added into Claim 1 and Claim 12.

Claim 11

Claim 11 has been cancelled.

Claim 12

Claim 12 has been amended to include limitations of Claim 10. Claim 12 discloses a single memory and memory controller both utilized by a servo control and ECC decoder circuit and a graphics decoding circuit for data reading and writing, whereas Cho does not disclose the aforementioned limitations (as detailed in the response to Claim 1). Furthermore, Claim 12 claims an electronic circuit fabricated on a monolithic substrate, namely that the claimed circuit components are formed on a monolithic substrate that enables communication between all circuit components. However, Cho does not disclose these limitations (as detailed in the response to Claim 1). For at least these reasons, the applicant asserts that Claim 12 should be found allowable over the prior art.

5. Claim Rejections – 35 U.S.C. 103(a)

Claims 15 – 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cho and Romano et al. and further in view of Iwamura.

Response

Claims 15 – 17 are dependent on Claim 12. As the applicant believes Claim 12 has been placed in a position for allowance claims 15 – 17 should also be found allowable.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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